Abstract of the Disclosure

An apparatus and method for using self-timing logic to make at least two accesses to a memory core in one clock cycle is disclosed. In one embodiment of the invention, a memory wrapper (28) incorporating self-timing logic (36) and a mux (32) is used to couple a single access memory core (30) to a memory interface unit (10). The memory interface unit (10) couples a central processing unit (12) to the memory wrapper (28). The self-timing architecture as applied to multi-access memory wrappers avoids the need for calibration. Moreover, the self-timing architecture provides for a full dissociation between the environment (what is clocked on the system clock) and the access to the core. A beneifical result of the invention is making access at the speed of the core while processing several access in one system clock cycle. In accordance with another aspect of the invention, the apparatus and method for using self-timing logic to make at least two accesses to a memory core in one clock cycle is incorporated into a data processing system, such as a digital signal processor (DSP) (40). In another embodiment of the invention, a memory core (26 embodied within RAM 206) incorporating the self-timing architecture is incorporated directly into the processor core thereby avoiding the need for a memory wrapper and the time delay associated with passing information from the processor core via the memory interface unit and to the memory core. Direct incorporation of a memory core into the processor core facilitates more intensive accessing and additional power savings.In accordance with yet another aspect of the invention, the apparatus and method for using self-timing logic to make at least two accesses to a memory core in one clock cycle is incorporated into a data processing system, such as a digital signal processor (DSP) (40, 190) is further incorporated into an electronic computing system, such as a digital cellular telephone handset (226).